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10/772,838	02/05/2004	Keith B. Hardin	2003-0116.02	6013

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EXAMINER	
ZHENG, EVA Y	
ART UNIT	**PAPER NUMBER**
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/772,838	HARDIN ET AL.	
	Examiner	Art Unit	
	Eva Yi Zheng	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,7-10,16-19,23-25* is/are rejected.

7)☒ Claim(s) *2-6,11-15 and 20-22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a) because they fail to show a demodulating circuit as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 2, 11 and 21 are objected to because of the following informalities:

a) Regarding to claims 2 and 11,

a) on line 5, please change "said transitions" to – transitions--, in order to avoid lack of antecedent basis.

b) on line 8, please change "said step" to – the step --.

c) on line 13, please change "said repeat cycles" to – repeat cycles---.

d) on line 16, please change "pattern set" to – pattern sets --.

b) Please review claim 21 for similar informalities.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 9, 19, and 21 are rejected under 35 U.S.C. 112, second paragraph, as being lack of antecedent basis.

(a) Claim 9 recites the limitation "said processing circuit" in line 2. There is insufficient antecedent basis for this limitation in the claim.

(b) Claim 19 recites the limitation "said first counter" and 'said second counter" in line 2. There is insufficient antecedent basis for this limitation in the claim.

(c) Claim 21 recites the limitation "said modulation pattern set" in line 13. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 7, 9, 10, and 16 are rejected under 35 U.S.C. 102(b) as being unpatentable by Asano et al (US 5,793,988).

a) Regarding to claim 1, Asano disclose a method for reducing electromagnetic emissions of data signals, said method comprising:

(a) providing a controller (enable signal in Fig. 2) having a first input (DATA in Fig. 2), a modulating circuit (100 in Fig. 2), and a first output (output of 130, X DATA in Fig. 2);

(b) providing a demodulating circuit (200 in Fig. 2), having a second input (input to block 200 and also the first input to block 220 in Fig. 2), and a second output (output of 230, X DATA in Fig. 2);

(c) providing a data pathway between said first output and said second input (interface cable 30 in Fig. 2);

(d) receiving an input data signal at said first input (DATA in Fig. 2);

(e) repetitively modulating, at said modulating circuit, said input data signal according to a predetermined modulation cycle (counter 110 in Fig.2), in which said modulation cycle comprises at least one modulating pattern set (Fig. 2 and 3 and Col 5, L1-41), thereby generating a first output data signal that is directed to said first output

(Fig. 2);

(f) transmitting said first output data signal from said first output to said data pathway (30 in Fig. 2);

(g) receiving said first output data signal from said data pathway at said second input (Fig. 2); and

(h) demodulating, at said demodulating circuit, said first output data signal, thereby generating a second output data signal that is directed to said second output, wherein a data content of said second output data signal corresponds to a data content of said input data signal (abstract).

b) Regarding to claims 7 and 16, Asano disclose wherein said controller operates in at least one of a plurality of selectable modes, as follows:

(a) a normal data signal mode without modulation;

(b) a divide by 2 mode without modulation;

(c) a data signal mode with modulation (Col 4, L51-67); and

(d) a divide by 2 mode with modulation.

d) Regarding to claim 9, Asano disclose wherein said processing circuit comprises one of:

a logic state machine, a sequential processor device, a parallel processor device, and discrete logic elements (N-bit counter in Fig. 2 constitutes as logic state machine or sequential processor device).

e) Regarding to claim 10, Asano disclose a method for reducing electromagnetic emissions of data signals, said method comprising:

(a) providing a controller (enable signal in Fig. 2) having an input (DATA), a modulating circuit (100), and an output (output of 130, X DATA);

(b) receiving an input data signal at said input (DATA);

(c) repetitively modulating, at said modulating circuit, said input data signal according to a predetermined modulation cycle (counter 110), in which said modulation cycle comprises at least two modulating pattern sets(first modulating pattern is counter increments Col 5, L59-Col 6, L2; second modulating pattern is counter decrements Col 6, L27-38) , thereby generating an output data signal that is directed to said output (Fig. 2).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Asano et al (US 5,793,988) in view of Ling et al (US 5,977,898).

a) Regarding to claim 8, Asano disclose a demodulating circuit that comprises an n-bit counter, adder and all the subject matters above except for the specific teaching of wherein the demodulating circuit comprises one of (a) an exclusive-OR gate, and (b) exclusive NOR gate.

However, Ling et al. disclose an adder circuit comprise an exclusive OR gate (XOR) (410 in Fig. 4). It is well known that an n-bit adder circuit comprises a plurality of logic gates including XOR. Therefore, it is obvious to one of ordinary skill in art to combine the teaching of demodulating circuit of Asano et al with the n-bit adder design of Ling et al. By doing so, provide decision selection and fast response in an n-bit adder.

9. Claims 17-19, 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asano et al (US 5,793,988) in view of Lo (US 6,026,141).

a) Regarding to claim 17, Asano disclose an electronic controller for reducing electromagnetic emissions of data signals, said controller comprising:

a first input that receives an input data signal (DATA in Fig. 2);

a modulating circuit (100 in Fig. 2), comprising:

a processing circuit that counts a number of transitions of a predetermined type of said input data signal, and that counts a number of repeat cycles of said transitions, and generates a modulation control signal (counter 110, Col 5, L1-Col 6, L39);

a plurality of logic gates that receive said modulation control signal, and said data input signal (adder 120, though not shown explicitly, it is well known that an adder comprises logic gates and multiplexers), and manipulate said data input signal in a manner that generates concentrations of electromagnetic energy emissions near a frequency of said data input signal (abstract; Fig. 11A and 11B), thereby creating a first output data signal (output of 130, X DATA); and

a first output that transmits said first output data signal (output of 130, X DATA and interface cable 30).

Asano disclose modulating circuit comprises an n-bit counter, adder and all the subject matters above except for the specific teaching of wherein the modulating circuit comprises multiplexers.

However, Lo disclose a typical multiple bit counter wherein comprises a plurality of multiplexers (6 in Fig. 3) It is well known that an n-bit counter circuit comprises a plurality of logic gates including multiplexers. Therefore, it is obvious to one of ordinary skill in art to combine the teaching of modulating circuit of Asano et al with the n-bit counter design of Lo. By doing so, provide fast response and decision in an n-bit counter.

b) Regarding to claim 18, Asano disclose wherein said transition of a predetermined type of said input data signal comprises one of:

(a) a rising edge transition (increments, Col 5, L59-67; Fig. 9); and

(b) a failing edge transition (decrements, Col 6, L27-39; Fig. 9).

c) Regarding to claim 19, Asano disclose wherein a counter element comprises at least one of:

(a) a hardware counter circuit (110 in Fig. 2);

(b) a register that is loaded and unloaded by way of a separate hardware circuit; and

(c) a memory element that is controlled by a processing circuit (120 in Fig. 2).

d) Regarding to claim 23, Asano disclose wherein said processing circuit comprises one of:

a logic state machine, a sequential processor device, a parallel processor device, and discrete logic elements (N-bit counter in Fig. 2 constitutes as logic state machine or sequential processor device).

e) Regarding to claim 24, Asano disclose a receiver circuit having a second input (input to 200 in Fig. 2) and a second output (X DATA in Fig. 2), and a data pathway between said first output and said second input interface cable 30 in Fig. 2);

wherein (a) said data pathway receives said first output data signal from said first output and directs it to said second input, and (b) said receiver circuit demodulates said first output data signal, thereby generating a second output data signal that is directed to said second output, wherein a data content of said second output data signal corresponds to a data content of said input data signal (Fig. 2).

10. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Asano et al (US 5,793,988) in view of Lo (US 6,026,141), further in view of Ling et al (US 5,977,898).

a) Regarding to claim 25, Asano disclose a receiver circuit that comprises an n-bit counter, adder and all the subject matters above except for the specific teaching of wherein the demodulating circuit comprises one of (a) an exclusive-OR gate, and (b) exclusive NOR gate.

However, Ling et al. disclose an adder circuit comprise an exclusive OR gate (XOR) (410 in Fig. 4). It is well known that an n-bit adder circuit comprises a plurality of logic gates including XOR. Therefore, it is obvious to one of ordinary skill in art to combine the teaching of receiver circuit of Asano et al and Lo with the n-bit adder design of Ling et al. By doing so, provide decision selection and fast response in an n-bit adder.

Allowable Subject Matter

11. Claims 2-6, 11-15, and 20-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eva Y Zheng whose telephone number is 571-272-3049. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eva Yi Zheng
Examiner
Art Unit 2611

May 18, 2007

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER